Design of Digital Signal Processor TMS320F28335 Stand Alone System for Real Time Application

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Abstract—*This paper presents the design of a new digital signal processing (DSP) stand alone evaluation board for real time application using TMS320F28335 DSP processor. A standalone evaluation board is a general purpose board with an embedded processor and generally with a way to download and execute user's program on it. The evaluation board is tested by implementing some DSP*
based algorithm to generate SPWM signal, used to drive the gate driver of IGBT. The algorithm development methodology and the experimental results are presented. The schematic and layout is designed using Eagle v6.1.0 PCB designer.

1. INTRODUCTION

The motivation and objective behind this paper was to create a standalone system which can be modeled as a general purpose system or an application specific system. Even different DSPs are available in the market, this standalone system developed as a product has greater advantages over them. Firstly, it gives more flexibility for the user in terms of I/O use as well as a multiprogramming approach. Even with such added options over the older one, the cost has drastically reduced. Unlike the control card and development board together accounting for $650 approx, this project required just $75. This results in a cost effective standalone system which is the need of the present day industry. This project is more than a project and acts like a product which can be used either as a development platform or used for an application specific system acting equivalent like ASIC (Application Specific Integrated Circuit).

2. DESIGN CONSIDERATION FOR DSP

During the phase of architecture selection, the hardware design of the whole system must also be taken into consideration. Surely, just considering the processor only is not enough for the selection. All the interfaces, communication paths with processors, hardware limitations, bottlenecks in the system and specific requirements of the hardware must also be taken into consideration. We design a board having 400MIPS DSP [1-2].

The consideration during design and implementation phases are presented below.

2.1 High Speed PCB Design

The term "high speed" can be misleading into believing that circuits with high clock frequency are high speed. It is the rise/fall time of a driving device that determines whether a circuit design can be termed high speed or not. Figure 1&2 shows signal integrity effects for a trace driven by two drivers with different rise/fall times. Apart from signal integrity, modern PCBs are also required to comply with rules on EMI/EMC [2,3]. Selection of number of layers, component placement and trace length are important parameters in PCB design. A related field known as "signal integrity analysis" subsumes transmission line effects, crosstalk and power/ground noise. In this section a theoretical overview of transmission lines effects, EMI/EMC considerations and use of decoupling capacitors is presented. Looking ahead, few of the output drivers on TMS320F280X series have a minimum rise/fall time of 2ns [2-4]. Hence a review of transmission lines is pertinent to this discussion.

2.2 Transmission Line Analysis of PCBs

A transmission line may be defined as any pair of conductors that is used to guide energy in the form of an electromagnetic field from one place to another. Electromagnetic field as the name suggests has two components, an electric and magnetic field, the two fields being at right angles to each other. The voltage difference between the transmission line trace and the surrounding planes is a measure of the strength of the electric field. The magnitude of current flowing in a transmission line is a measure of the strength of the magnetic field. Hence a PCB can be seen as flow of electromagnetic fields from point to point. Ensuring that this electromagnetic field does not exit the board and interfere with external devices is the topic of discussion on EMI [3-4].

2.2 PCB design with EMI/EMC considerations

The techniques used to ensure signal integrity are closely related to guidelines for EMI compliance. It is important to understand that software and hardware tools that test a PCB for EMI/EMC compliance is an extensive field. As mentioned earlier, a PCB circuit can be seen as flow of electromagnetic energy from point to point. Under certain circumstance, a part of the energy can amplify and exit the board when flowing through traces with a specific geometry [5-7].

Summarizing, EMI can be reduced with the following:

1) High frequency traces must be kept as short as possible (example clock signals).

2) Signal traces must be close to a ground plane, to reduce loop area of the signal. Ensuring that only differential signals exists, automatically minimizes or eliminates common mode signals.

Best EMI reduction can be achieved by having every signal layer associated with a ground layer beneath it.

3) The ground plane must be solid without too many discontinuities due to vias.

4) All sources of parasitic inductance must be minimized. (example sockets, leads of components etc).

The other factors key to a good PCB design are listed below.

1) Board layer selection
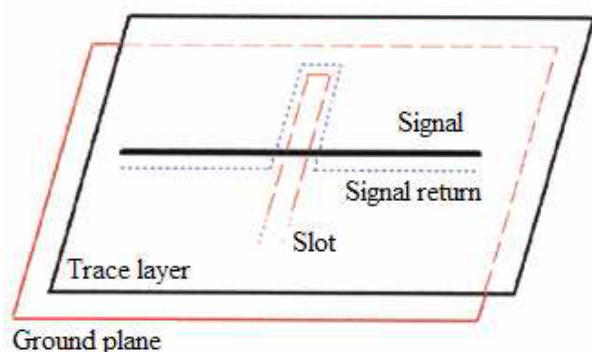
2) Component placement

3) Decoupling capacitor

Fig. 1: Routing a trace over a slot in a plane can cause large loop area

2.3 Board Layer Selection

The Selection of the number of layers for a PCB depends on a number of factors like

a) Complexity of schematic: The number of nets or connections in the circuit and the number of components.

b) Type of components: Surface mount devices, especially fine pitch devices have high density of pins and hence it becomes nearly impossible to route them on a two layer board.

c) Trace width: If the circuit requires high currents, trace widths must be wider, hence occupying more space on the board.

d) Real estate constraint: This is generally considered the prime motive for layer selection. It is possible to reduce the size of the board by increasing the number of layers.. More number of layers provides the extra degree of freedom in routing, allowing components to be place closer and hence shorter trace lengths.

e) Cost: Since higher number of layers provides extra latitude in routing and also better EMI suppression, one might be tempted to be use it more frequently. But they cost much more than boards with lesser layers and hence must be considered in the design stage.

2.4 Component Placement

Optimal placement of components is one of the most important steps in PCB design. In the section on EMI considerations, emphasis was placed on having small loop currents. This can be achieved by placing functionally related components together. When placing components the length of traces must be estimated in high speed design. If the traces exceed the maximum permissible length to prevent transmission line effects, then termination resistor values must be calculated and updated in the schematic. If the circuit has analog and digital circuitry, it is necessary to functionally separate the two modules. A separate analog and digital ground is not necessary. Since the return signal generally follows the path beneath the trace, the analog and digital sections are partitioned such that none of the signals cross each other. Hence good routing discipline can prevent contamination of analog and digital signals with a single ground plane.

3. HARDWARE DEVELOPMENT

Step by step board design has been presented below considering all the hardware considerations.

3.1 Circuit Design and Schematic Explanation

3.1.1 Power module

The TMS320F28335has various power supply pins for different individual modules. This includes:

- CPU core supply (VDD)

- I/O supply (VDDIO)

- ADC analog supply pins (VDDA2, VDDAIO)

- ADC core supply (VDD1A18, VDD2A18)

- Flash programming voltages (VDD3VFL)

- Supply ground (VSS, VSSIO)

- ADC analog ground (VSSA2, VSSAIO)

All the power supply pins must be connected for proper operation. All these devices have multiple supply pins for the core, I/O, and ADC/analog supplies. All such pins must be connected to the proper supply voltage for proper operation. The voltage level for I/O pins is 3.3 V; whereas, the core supply voltage is 1.8 V or 1.9 V. They also have Flash programming supply pins. These pins have to be connected to 3.3 V rail, particularly for in-circuit flashing applications. For dual voltage regulator we are using TPS767D01. The TPS767D01 is a dual voltage regulators which provides 1.8V-1.9V and 3.3V with fast transient response, low dropout voltages and dual outputs in a compact package and incorporating stability with low ESR output capacitors [8-12]. The schematic for power module is shown below in fig.2.
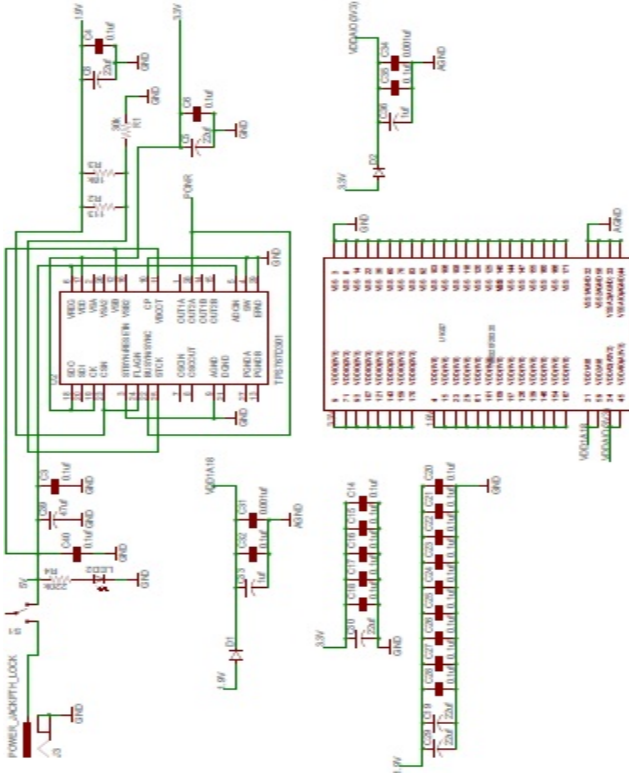

Fig. 2: Schematic for Power Supply

3.1.2 Bypass Capacitors

Like most of the TI DSPs, C2000 parts are fabricated using advanced CMOS technology, which gives good high-speed performance consuming little power. The CMOS circuits draw large currents at every transition, producing current spikes on the supply rails. These rising and falling glitches have to be filtered before they traverse into the sensitive circuit area. The bypass or decoupling capacitors placed across supply-positive pins and ground are used for such filtering; F28x DSCs have

several supply-positive pins. We need to use one capacitor on each supply-positive pin and should place this capacitor as close to the pin as possible, without using any via. Typically small (10 nF to 100 nF), low-ESR ceramic capacitors are used for this purpose [6-7].

3.1.3 Generating Analog Supply from the Digital Supply

For most of the applications, the current drawn by the analog circuitry is small compared to the digital parts and it is okay to have a single voltage regulator capable to provide enough current for both type of parts. However, we need to isolate the analog supply from the noisy digital supply rail. The simplest form of circuit for generating an analog supply from the digital rail is to use passive components such as inductors to filter out the noise components. The inductors act as low pass filters, letting the DC power supply component through, but choking the noise, which is usually at a fairly high frequency. Using Ferrite beads is a better choice over a standard inductor. Ferrite beads have negligible parasitic capacitance; the electrical characteristics are similar to inductor [8,9].

3.1.4 Clock Module

The TMS320F28335 devices offer two options for clock generation: using an onboard crystal oscillator or feeding the external clock to the XCLKIN pin or X1 and X2 pin. The frequency of this basic input clock, using an internal oscillator, is in the range of 20 MHz-35 MHz. The on-chip phase-locked loop (PLL) can be set to multiply the input clock to provide a wide variety of system clock frequencies. To select a proper external oscillator, consider the specifications such as frequency, stability, aging, voltage sensitivity, rise and fall time, duty cycle, and signal levels. Some designs may have to consider clock jitter.TMS320F28335 devices can accept an external clock signal having an amplitude of VDD (1.8 V/1.9 V) or 3.3 V [10-12]. The schematic for clock module is shown in fig.3.
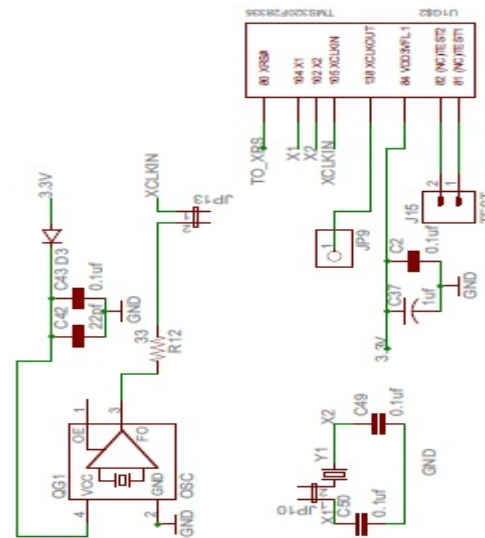

Fig. 3: Schematic for clock module

3.1.5 JTAG Module

JTAG, as defined by the IEEE Std.-1149.1 standard, is an integrated method for testing interconnects on printed circuit boards(PCBs) that are implemented at the integrated circuit level. The JTAG test architecture provides a means of test interconnects between integrated circuit board without using any physical probes. It adds a boundary-scan cell that includes a multiplexer and latches to each pin on the device. Boundary-scan cells in a device can capture data from pin or core logic signals, or force data onto pins. Captured data is serially shifted out and externally compared to the expected results. TMS320F28335 use five of the standard IEEE Standard1149.1–1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (JTAG) signals (TRST,TCK, TMS, TDI, and TDO) and two of the TI extensions (EMU0 and EMU1). A transient voltage suppressor arrays PACDN042 is used which provides a very high level of protection for sensitive electronic components that may be subjected to electrostatic discharge (ESD). The PACDN042/43/44/45/46 devices safely dissipate ESD strikes, exceeding the IEC 6100042 International Standard, Level 4 (8 kV contact discharge) [8-12].The Schematic for JTAG module is shown in fig.4.
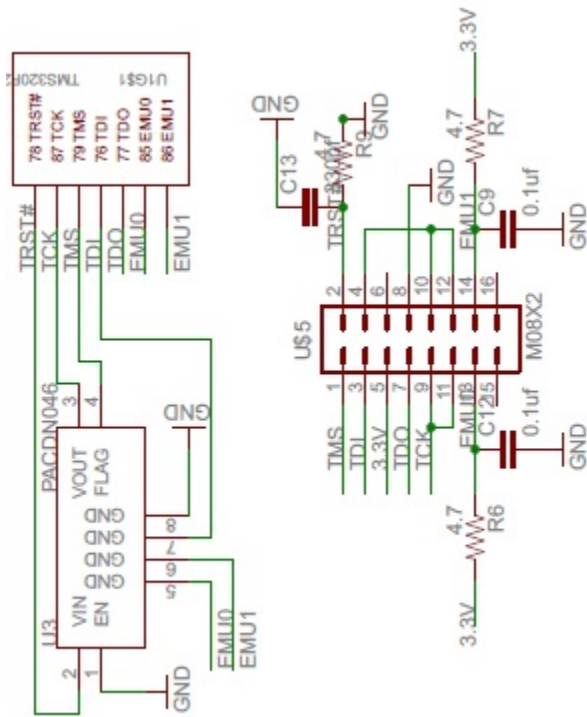

Fig. 4: Schematic for JTAG module

3.1.6 ADC Input Module

The ADC peripheral requires few external components for biasing of internal band gap reference and filtering noise on reference voltage signals. The schematic in Figure 10 shows these parts and their connections. All the ADC blocks of the F28xx/F28xxx devices have internal band gap reference voltage source. Connecting an external voltage reference for TMS320F28335 devices, the ADC blocks of these parts require a single reference voltage input to be connected between the ADCREFIN and ADCLO pins. The ADC logic can be supplied by an external voltage reference. The TMS320F28335 ADC accepts 2.048 V, 1.5 V, or 1.024 V on the ADCREFIN pin. We also need to set a two-bit field of the ADC Reference Select Register (ADCREFSEL) according to the voltage level of the external source to enable the external reference and determine the reference source selected [8-12]. The Schematic for ADC module is shown in fig.5.

3.1.7 GPIO Module

The GPIO pins are multiplexed for two or more signals; each GPIO pin could be used to implement digital I/O or peripheral I/O. To help the routing of signals or if you need to use the pin for a different multiplexed option, some of the peripheral signals are multiplexed at two different sets of pins. The drive strength (sink/source current) of the output buffer on GPIO pins is typically 4 mA (unless otherwise noted). The maximum toggling frequency of the GPIO pin is 25 MHz. At reset, the GPIO pins are defined as input (default condition).All of the F28x devices are built around CMOS technology. Therefore, either configured as outputs and left unconnected or define them as input with proper termination on the pin. A pullup or pulldown resistor (1 kΩ to 10 kΩ) to VCC or GND puts them in defined state [8-12]. The Schematic for GPIOs is shown in fig.6.
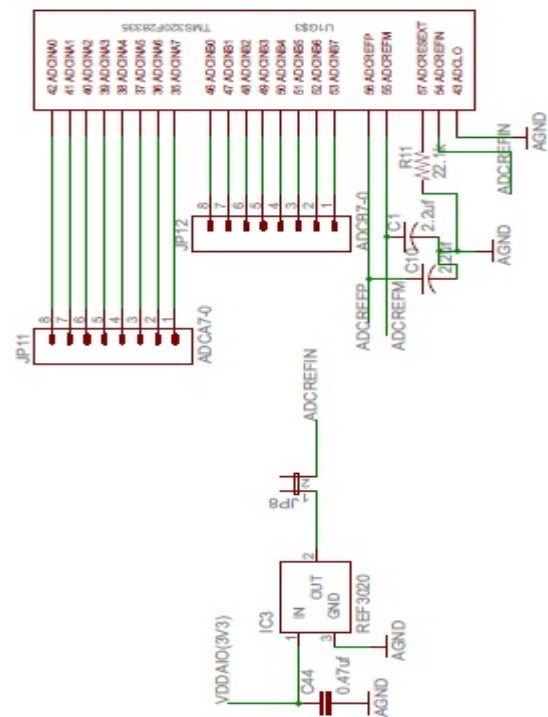

Fig. 5: Schematic for ADC module

3.1.8 RESET Module

The XRS pin facilitates the device reset (in) and watchdog reset (out) signals. A warm reset pulse-width is specified as eight times the oscillator clock (OSCCLK) period; however, the power on reset's pulse-width has to be much longer to account for the time required for VDD to reach 1.5 V (to enhance Flash reliability) and the oscillator start-up period of 10 ms (nominal). We prefer to keep this duration in excess of 100 ms to overcome any other related delays. During power down, the XRS pin must be pulled low at least 8 μs prior to VDD reaching 1.5 V to enhance flash reliability. Whenever the 8-bit watchdog up counter has reached its maximum value, the watchdog module generates an output pulse 512 oscillator clocks wide. The WDRST signal outputs the reset signal over the XRS pin. The output buffer of this pin is an open-drain with an internal pullup (100 uA, typical) [8-12].

3.1.9 Serial Communication /RS232 Module

I2C and serial peripheral interface (SPI) are board-level interfaces that are connected to other devices on the board or system. These signals normally run directly. SCLA and SDAA pins of the I2C link are required to be pulled high using a 5 KΩ resistors. However, serial communications interface (SCI) and controller area network (CAN) interfaces are used to connect to different systems running under another processor. These ports require specialized transceiver parts to transform the signal into the required electrical signaling (single-ended RS232 or differential for CAN and RS422/RS485), so that they can interface with the ports on the other devices per defined protocol. The MAX3243 is a multi channel RS232 line drivers/receiver, with 15-kV ESD (HBM) protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The device operates at data signaling rates up to 250 kbit/s and a maximum of 30-V/s driver output slew rate [8-12]. The Schematic for RS232 interface has been shown in fig.7.

Fig. 6: Schematic for GPIO module

Fig. 7: Schematic for MAX3243 module

3.1.10 Boot-Mode and Flash Programming Options

All F28x devices come with a factory programmed Boot-ROM that contains bootloading software and standard tables,

such as SIN/COS waveforms for use in math related algorithms. The first consideration is to tell the bootloader software which Boot mode to select at power on. Another point to consider is the Flash-programming mode at production level.

3.2 Physical Layout Design

In the above section, information relevant to each peripheral that affects the schematic designs was discussed. It was determined that they need external circuitry for their proper functioning. Analog signal conditioning and power supply topics were also covered. The other important parts on the schematics are bypass capacitors and connectors. Component placement and layout design are quite challenging tasks. The component placement and board design are shown in fig.8.

3.2.1 Placement Planning

The way we arrange our components has a huge impact on how easy or hard the next step will be. As we're moving, rotating, and placing parts, there are some factors we should take into consideration:

- Avoiding overlapping of components: All of our components need some space to breathe. The green via holes need a good amount of clearance between them too.

- Minimizing intersecting airwires: While moving components, we must have an eye on how the airwires move with them.

- Component placement requirements: Some components always require special consideration during placement. For example, DB9 connector must be facing the edge of the board. And also that decoupling capacitor is nice and close to the IC.

- Tighter placement means a smaller and cheaper board, but it also makes routing harder.

3.2.2 Routing the Board

Routing is the most challenging part of this entire process. Our job is to turn each of those gold airwires into top or bottom copper traces. At the same time, we also have to make sure not to overlap two different signals. To draw all of our copper traces, we'll use the ROUTE tool (not the WIRE tool). After selecting the tool, there are a few options to consider on the toolbar given below. And hence the final routed board has been shown in fig.9.

3.2.3 Manufacturing the Board

After the final board designing, it's time to place the order to a good PCB manufacturer. Before they fabricate the board, the fabrication house usually run a quick design for manufacturability (DFM) check, and let us know if something on our design will cause in a problem. Finally the board was fabricated and has been shown below in fig.10
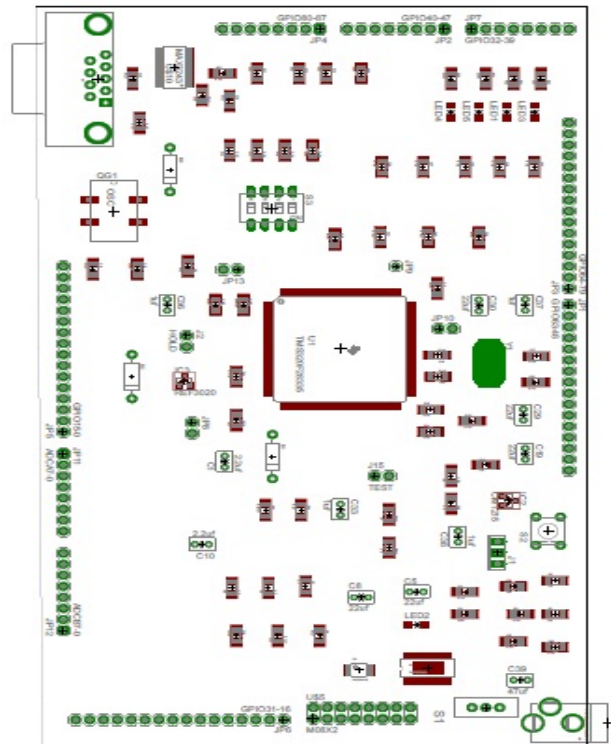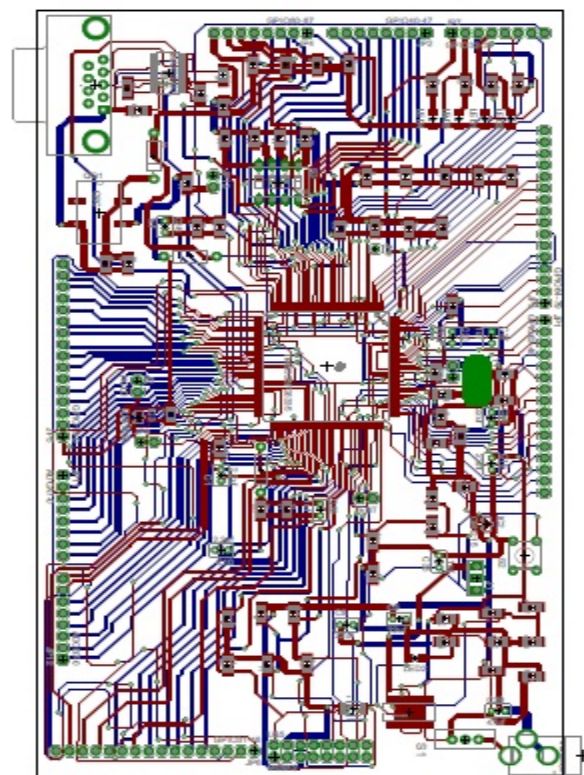

Fig. 8: Component Placement

Fig. 9: Complete Routed Board

Fig. 10: Fabricated Board

Fig. 11: Finalized DSP Board

Finally the fabricated board is checked manually for any routing error. And the next step is to mount the components on the board. A great care has been taken while mounting the SMD components, due to its delight pins and temperature considerations. The fig.11 below shows the final component placement on the DSP board.

3.3 Hardware cost calculation

The overall cost of the DSP board depends on the number of boards build at the same time. Let's assume a total of three boards in the following. The exemplary calculation in Table.1 provides an overview of the expected costs per module.

Table 1: Hardware Cost Calculation

Components	Manufacturer	Cost per unit (US $)
TMS320F28335	Texas Instruments	17
TPS767D301	Texas Instruments	5
REF3020	Texas Instruments	0.5
PACDN046	Texas Instruments	3
CM1215	Texas Instruments	0.5
MAX3243	Texas Instruments	3
Resistors & Capacitors	Local	3
Connectors	Local	3
Miscellaneous	Local	5
Board Fabrication	Yashna Circuits, Mumbai	35
Total		75

4. EXPERIMENTAL RESULTS & CONCLUSION

After the successful testing of DSP board, a real time application from the field of power electronics has been successfully tested on the board. In this paper the design and development of an embedded DSP controller was presented. The DSP board was designed to use all the features of the TMS320F28335.

The integration of power application devices like inverters, DC/DC converters on a single DSP controller board is an area for future work. This will involve careful considerations for separating power signals from electronic high frequency of the DSP.

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